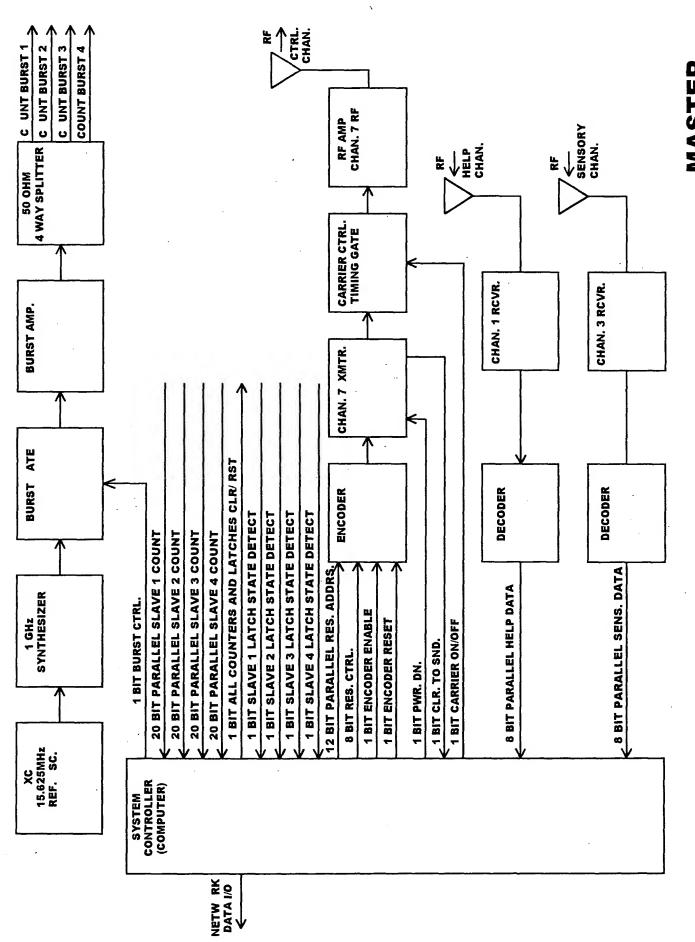
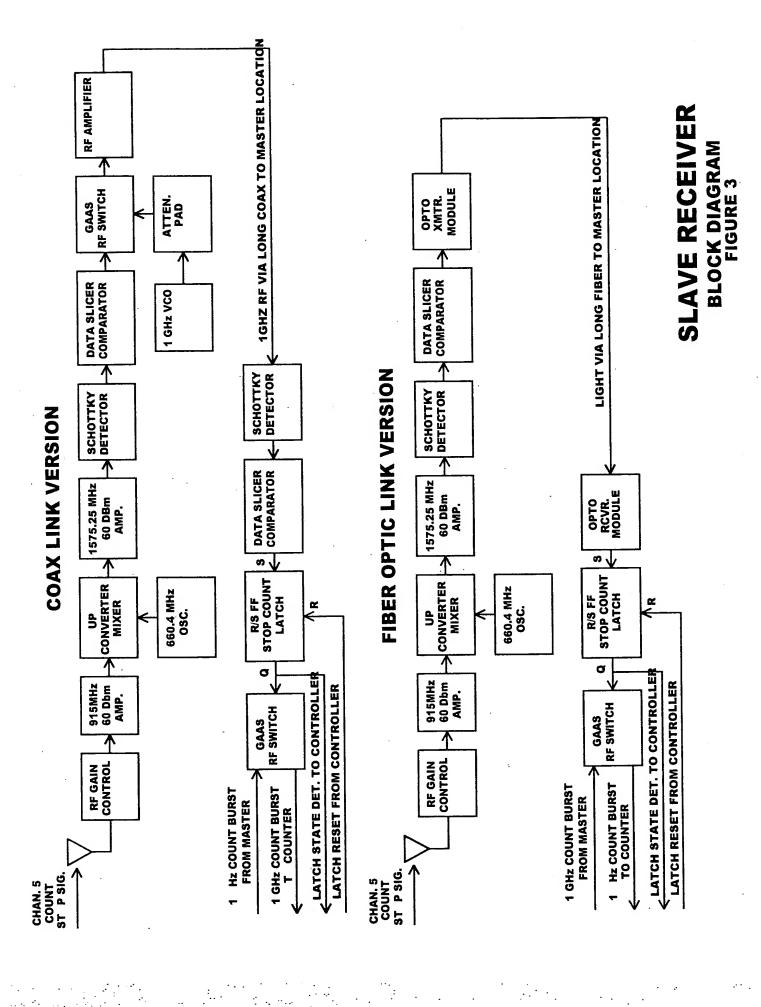
NETWORK DATA 1/0 REF. BURST AMP REF. BURST SPLITTER CHAN 7 ENCODER/XMTR. CHAN 1 RCVR./DECODER PRECISION REF. SOURCE REF. BURST GATE SYSTEM CONTROLLER NETWORK I/O MODEM CHAN 3 RCVR, DECODER (FI URE 2) **COUNTER RESET COUNT BURST** LATCH STATE DETECT LATCH RESET COUNT DATA 20 BIT CHAN 7 RF LINK ADDR/CTRL/START SEQ. COMPARATOR STOP COUNT LATCH LOGIC TRANSLATOR 12 BIT TTL COUNTER 8 BIT ECL COUNTER FIBER OPTIC RCVR. SLAVE RECEIVER COUNTER GATE SLAVE COUNTER RF COAX. RCVR. (FI URE 3) DETECTOR CHAN 3 RF LINK SENSORY DATA (FIGURE 4) **GATED COUNT BURST** CHAN 1 RF LINK CALL HELP FIBER OPTIC OR RF LINK (LONG DX) STOP SLAVES COUNT **CHAN 5 RF LINK** CHAN 1,3,5 XMTR. PIC C NTROLLER 1 RF TIMING SWITCH SENSORY MODULE RESIDENT MODULE CHAN. 5 RCVR. FIBER PTIC XMTR PIC C NTROLLER 2 MICROPROCESSOR RF TIMING SWITCH SLAVE RECEIVER (FI URE 3) RF C AX XMTR CHAN. 7 RCVR. CHAN 5 XMTR. CHAN. 7 RCVR. (FI URE 5) FLASH RAM (FIGURE 6) CAL. UNIT DECODER DECODER ENCODER

LAPS BASIC SYSTEM BLOCK DIAGRAM FIGURE 1



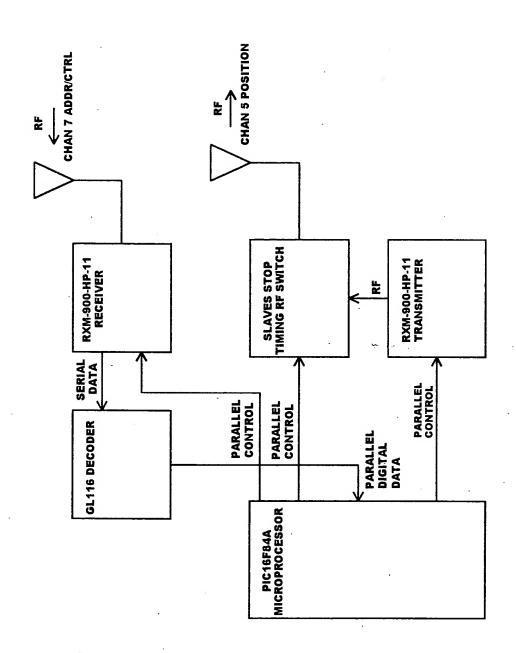
MASTER BLOCK DIAGRAM FIGURE 2



12 BIT MSB COUNT TO MASTER 8 BIT LSB COUNT TO MASTER CARRY BIT 12 BIT TTL BINARY COUNTER ECL T TTL TRANSLATOR 8 BIT ECL 8 BIT ECL BINARY COUNTER COUNTER RESET FROM MASTER 1 GHz COUNT BURST FROM SLAVE RECEIVER

SLAVE COUNTER BLOCK DIAGRAM FIGURE 4

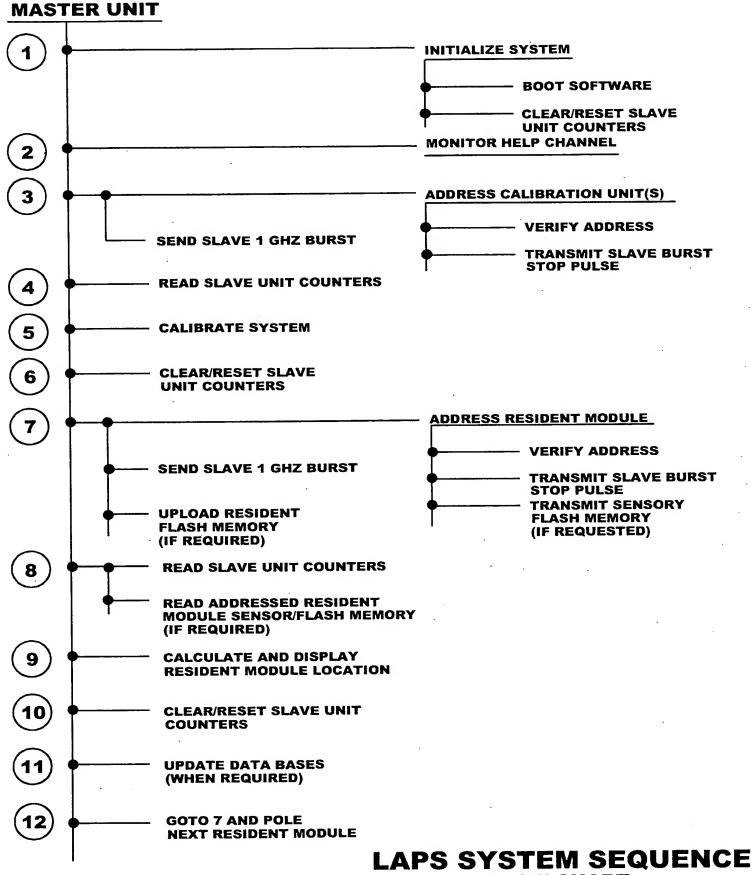
CALIBRATION UNIT BLOCK DIAGRAM FIGURE 5



CHAN 5 POSITI CHAN 3 DATA CHAN 1 HELP CHAN 7 ADDR/CTRL SLAVES STOP TIMING RF SWITCH RXM-900-HP-11 TRANSMITTER RXM-900-HP-11 RECEIVER SERIAL DATA SERIAL DATA PARALLEL CONTROL PARALLEL CONTROL PARALLEL CONTROL **GL116 DECODER** PARALLEL DIGITAL DATA PIC16F84A MICROPROCESSOR PARALLEL MEMORY ADDR. PARALLEL CTRL/DATA DATA TO TX SENS RY M DULE MICROPROCESSOR DATA ENCODER SENSORY RCVR. FLASH RAM SENS. DATA RESIDENT

F

RESIDENT MODULE BLOCK DIAGRAM FIGURE 6



LAPS SYSTEM SEQUENCE FLOW CHART FIGURE 7